

QNX BSP for QBlissA9

FULL Version

by IBV - Echtzeit- und Embedded GmbH & Co. KG

Subject: Release Notes (**PRELIMINARY**)
 Version: 1.0, QNX 6.5.0SP1
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1. Features

1.1. Components of the BASE Version of the BSP

Component	Format	Features, Notes
Startup (BASE version)	Source	<ul style="list-style-type: none"> ◆ Configurable DDR3 RAM size ◆ Supports QNX SMP
Serial	Source	<ul style="list-style-type: none"> ◆ QNX character device driver (devc-) ◆ Supports i.MX6 UART2 (Qseven signals 185...188) ◆ Supports i.MX6 UART3 (Qseven signals 161...164) ◆ RTS/CTS handshake supported ◆ Driver is interrupt driven (no DMA support)
FEC Network	Source	<ul style="list-style-type: none"> ◆ QNX network driver DLL for io-pkt network stack (devnp-) ◆ Supports i.MX6 Gigabit Ethernet Controller ◆ Support Ethernet PHY in RGMII mode on QBlissA9 module, limited to Ethernet interfaces MDIO and MD11 (Qseven signals 9...12) ◆ 10/100 MBit speed ◆ Half / full duplex mode ◆ MAC address is used from uboot environment

1.2. Components of the FULL Version of the BSP

Component	Format	Features, Notes
Startup (FULL version)	Source	<ul style="list-style-type: none"> ◆ Configurable DDR3 RAM size ◆ Supports QNX SMP
SD	Source	<ul style="list-style-type: none"> ◆ QNX file system driver (devb-) based on QNX MMC driver framework ◆ Supports i.MX6 uSDHC3 Controller ◆ Driver is interrupt driven (no DMA support)
USB	Binary	<ul style="list-style-type: none"> ◆ QNX USB driver DLL for io-usb USB stack (devu-) ◆ Supports i.MX6 USB Host1 Controller (EHCI) with USB PHY2 in high speed mode ◆ Supports USB hub on QBlissA9 module (QSeven signals 96, 94, 90, 88) <p><u>Driver is shipped as original binary as provided by the operating system vendor in the original i.MX6 reference BSP and without support.</u></p>

I2C	Source	<ul style="list-style-type: none"> ◆ QNX I2C master driver (i2c-) ◆ Supports i.MX6 I2C1 Controller in master mode (Qseven signals 60, 62) ◆ Supports i.MX6 I2C2 Controller in master mode (QBlissA9 on-board I2C devices) ◆ Supports i.MX6 I2C3 Controller in master mode (Qseven signals 66, 68)
SPI	Source	<ul style="list-style-type: none"> ◆ QNX SPI master driver based on QNX SPI Framework ◆ Supports i.MX6 ECSPi2 Controller in master mode (Qseven signals 199...203) ◆ QNX SPI master API library shipped as binary without support ◆ Supports transfers with 1...32bit in normal mode and 8 / 16 / 32bit transfers in burst mode ◆ Supports control of up to 2 slave select signals per SPI controller ◆ The driver is interrupt driven, DMA based transfers are not supported.
CAN	Source	<ul style="list-style-type: none"> ◆ QNX CAN driver based on QNX CAN Framework ◆ Supports i.MX6 FLEXCAN2 Controller (QSeven signals 129, 130) ◆ Supported baud rates: 20K, 25K, 50K, 100K, 125K, 250K, 500K, 1M ◆ Extension for transmission of CAN frames with payload sizes other than eight and remote frames ◆ Ready for use with EMBRICS ioCAN
SATA	Binary	<ul style="list-style-type: none"> ◆ QNX file system driver (devb-) ◆ Supports i.MX6 SATA Controller <p><u>Driver is shipped as original binary as provided by the operating system vendor in the original i.MX6 reference BSP and without support.</u></p>
PCIe	Source	<ul style="list-style-type: none"> ◆ QNX PCI driver (pci-) ◆ Supports i.MX6 PCIe bus ◆ Message Signaled Interrupts (MSI) are not supported by QNX
GRAPHICS	Source	<ul style="list-style-type: none"> ◆ QNX graphics driver DLL for io-display (devg-) ◆ Supports i.MX6 graphic controller for applications working with the QNX GF interface and QNX Photon ◆ Supported display interface: LVDS ◆ Configurable bit mapping (SPWG/JEIDA) for LVDS display ◆ Configurable display colour depth (18/24 bpp) ◆ Frame buffer access (no hardware acceleration) ◆ Configurable display resolution (supported pixel clock 6...85 MHz) ◆ Supported pixel formats: ARGB8888, RGB888, RGB565 <p>Limitations:</p> <ul style="list-style-type: none"> ◆ Only one IPU (IPU1) is supported ◆ Only one display interface (DI0) is supported ◆ Only one LVDS channel (LVDS0) is supported ◆ Only one graphics layer is supported ◆ There is no support for alpha-blending or chroma-keying

1.3. Optional Driver Modules (not part of FULL Version of the BSP)

GPIO		on request
TOUCH		on request
AUDIO		on request

1.4. Further BSPs for F&S Boards

A complete list of all available QNX Board Support Packages for embedded boards by F&S Elektronik Systeme GmbH is available at:

http://www.ibv-augsburg.net/media/pdf/QNX_BSP_Overview_FS.pdf

PRELIMINARY

2. General Information

2.1. Features of the BSP

The features of this Board Support Package and the Application Programming Interface (API) are defined and limited by the underlying QNX reference BSPs. Changes in the target system and/or peripheral components may require an adaption of the BSP. Therefore the BSP is provided in source code.

2.2. Dynamic voltage and Frequency Scaling (DVFS)

When running QNX, the CPU is clocked with the frequency selected by the boot loader "uboot".

Dynamic voltage and frequency scaling (DVFS) is not supported in QNX!

Important note:

Additional measures for cooling are necessary especially if more than one i.MX6 core is used. Without additional measures, the board may be damaged. Please discuss this issue with your board vendor.

3. Target System

- ◆ F&S QBlissA9 Qseven™ Modul with ARM Cortex™ A9 Single-/ Dual-/ Quad-Core
 - ◆ Freescale i.MX6 applications processor
 - ◆ 1 GB DDR3 RAM (size configurable)
 - ◆ Tested and released for 800 MHz clock
- ◆ F&S QBliss StartIntf Board, Rev. 1.3
- ◆ Operating system QNX 6.5.0 with SP1
- ◆ Boot loader U-Boot 2009.08-dirty (Sep 03 2013 - 11:32:38)

4. Host Development System

- ◆ QNX Software Development Platform 6.5.0SP1
- ◆ Terminal emulation program (Qtalk, Momentics IDE Terminal, tip, HyperTerminal, etc.)
- ◆ RS-232 serial port or a USB-to-serial adapter, and a straight-through serial cable
- ◆ Ethernet link

5. Known Issues for this BSP

- ◆ Ethernet driver: The maximum supported speed is 100MBit. See also i.MX6 Errata ERR004512, "ENET system limitation". As workaround there is an option in the Ethernet driver to limit auto negotiation speed to 100MBit.
- ◆ The PCIe driver uses the same PLL as the SATA controller, and resets it during PCIe initialization. Therefore, the PCIe driver must be started before the SATA driver.
- ◆ The PCIe driver supports one PCIe lane with one PCIe device. If an external bridge is placed on the custom hardware, an adaption of the driver may be necessary.

6. Change History

6.1. Revision 1.0

- ◆ CAN driver added to FULL Version, BASE Version is unchanged
 - ◆ Supports transmission of CAN frames with payload sizes other than eight
 - ◆ Support of remote frames
 - ◆ API distinguishes 11bit (CAN 2.0A) and 29bit (CAN 2.0B) identifiers
 - ◆ Byte order within the frames during send and receive is not changed
- ◆ Startup: configuration for SDRAM size added
- ◆ Bugfixes applied on i.MX6 QNX6 Reference BSP:
 - ◆ Serial driver: correct handling of line status
 - ◆ Network driver: Support auto negotiation with speed limit to 100 MBit/s
 - ◆ Network driver: Workaround for i.MX6 errata ERR006358 "ENET: Write to Transmit Descriptor Active Register (ENET_TDAR) is ignored"
 - ◆ SPI driver: support of different SPI transfer lengths and SPI message sizes
 - ◆ SPI driver: support of clock polarity and clock phase
 - ◆ SPI driver: support of SPI clock setting
- ◆ Adapted for QBlissA9 board

7. Sales / Technical Support

To get this BSP or to obtain technical support for the BSP, please contact:

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